In re Patent Application of:
MORIN ET AL.
Serial No. 10/701,165
Filing Date: November 4, 2003

REMARKS

Applicants appreciate the Examiner's careful and thorough examination of the present application. By this amendment, the claims have been amended to eliminate the alleged indefiniteness noted by the Examiner. Although Applicants respectfully disagree with the Examiner's position regarding the characterization of two layers defining an overall layer, the claims were amended to avoid the terminology and advance prosecution of the application. Accordingly, the amendment does not raise any new issues. Claims 12-38 remain pending in the application. Favorable reconsideration is respectfully requested.

I. The Invention

As shown in FIGS. 3-5, for example, the invention is directed to a semiconductor device having MOS transistors, and a method for fabricating the same, so that the residual stress level of an etch-stop layer is discriminately adapted to the type of transistors that it covers. This is provided by a semiconductor device, which comprises a semiconductor substrate in which MOS transistors are formed therein, a dielectric layer that covers the substrate, and a first etch-stop layer having a first residual stress level and covering some of the MOS transistors, and a second etch-stop layer of material having a different residual stress level and covering all of the MOS transistors.

II. The Claims are Patentable

Claims 12-38 were rejected in view of Lee et al. (U.S. Patent No. 6,372,569) taken alone or in various

combinations with En et al. (U.S. Patent No. 6,573,172) and Zheng et al. (U.S. Patent No. 6,762,085) for the reasons set forth on pages 2-11 of the Office Action. Applicants contend that Claims 12-38 clearly define over the cited references, and in view of the following remarks, favorable reconsideration of the rejections under 35 U.S.C. §102 and §103 is requested.

Independent Claims 12, 20 and 26 are directed to a semiconductor device including at least one first MOS (NMOS or PMOS) transistor and at least one second MOS (PMOS or NMOS) transistor in a semiconductor substrate. A dielectric layer is on the transistors, and a first etch-stop layer covers the at least one first MOS transistor and has a first residual stress level, and a second etch-stop layer covers the first and second transistors and has a second residual stress level different than the first residual stress level. Similarly, independent method Claim 32 recites forming a first etch-stop layer covering the at least one first MOS transistor and having a first residual stress level, and forming a second etch-stop layer covering the at least one first MOS transistor and the at least one second MOS transistor and having a second residual stress level different than the first residual stress level. It is these combinations of features which are not fairly taught or suggested in the cited references and which patentably define over the cited references.

The Lee et al. patent is directed to a method of selective formation of an SiN layer in a semiconductor device having at least one PMOS transistor and one NMOS transistor formed therein. An undoped silicate glass (USG) layer is deposited over the semiconductor structure and the PMOS and

NMOS transistors. A silicon nitride layer is deposited over the undoped silicate glass layer and over the PMOS and NMOS transistors. The silicon nitride layer is patterned, etched, and removed from over the PMOS transistor. An inter-level dielectric (ILD) layer is formed over the structure.

The Examiner has relied on the Lee et al. patent as allegedly disclosing an etch stop layer including the layers 52 and 50 in FIG. 7. Applicants maintain that the Examiner has misinterpreted the cited reference. Specifically, Applicants note that in Lee et al., only the liner layer 50 can be considered to be an etch stop layer. Indeed, there are no first and second etch stop layers as claimed.

As a matter of fact, according to the method of Lee et al., an oxide layer is deposited over NMOS and PMOS transistors after salicidation to form a gate salicide contact region. H_2-rich PECVD silicon nitride layer is then deposited over the oxide layer, over the NMOS and PMOS areas. A composite photo resist mask is then formed over NMOS transistor in the NMOS area. A nitride etch selective to the underlying oxide layer is then conducted to remove the unmasked H_2-rich PECVD nitride layer portions. The mask is thereafter removed to expose, on the one hand, remaining H_2-rich PECVD nitride layer portion and underlying the oxide layer portion over NMOS transistor.

A dielectric layer is then deposited and planerized and identified. During the identification step, the H_2-rich PECVD nitride layer portion acts as a solid source diffusions providing hydrogen to NMOS transistor, which decreases the I_{off} of NMOS transistor. Accordingly, in the Lee et al. patent, the PMOS transistors are covered by an oxide layer, and the NMOS

transistors are covered by the oxide layer 50 and the NMOS transistors are covered by the oxide layer 50 and by the silicone nitride layer 52.

In the semiconductor structure disclosed in Lee et al., the oxide layer 50 constitutes an etch-stop layer for the etch conducted to remove the nitride layer 52. On the contrary, the nitride layer is used as a solid source diffusion, providing hydrogen to the under lying NMOS transistors. Importantly, according to the claimed invention, the semiconductor device comprises a first etch-stop layer covering the first transistor and having a first residual stress, and a second etch -stop layer covering the first and second transistors and having a second residual stress level different than the first residual stress level.

As the Examiner is aware, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. The identical invention must be shown in as complete detail as is contained in the claim.

The En et al. and Zheng et al. references were cited to teach the use of various residual stress levels of layers in MOS transistors. Without discussing these references in detail, in is sufficient to note that nothing therein makes up for the deficiencies of the Lee et al. patent as pointed out above.

There is simply no teaching or suggestion in the cited references to provide the combination of features as claimed. Accordingly, for at least the reasons given above, Applicants maintain that the cited references do not disclose or fairly suggest the invention as set forth in Claims 12, 20,

26 and 32. Furthermore, no proper modification of the teachings of these references could result in the invention as claimed. Thus, the rejections under 35 U.S.C. §102(e) and §103(a) should be withdrawn.

It is submitted that the independent claims are patentable over the prior art. In view of the patentability of the independent claims, it is submitted that their dependent claims, which recite yet further distinguishing features are also patentable over the cited references for at least the reasons set forth above. Accordingly, these dependent claims require no further discussion herein.

III. Conclusion

In view of the foregoing remarks, it is respectfully submitted that the present application is in condition for allowance. An early notice thereof is earnestly solicited. If, after reviewing this Response, there are any remaining informalities which need to be resolved before the application can be passed to issue, the Examiner is invited and respectfully requested to contact the undersigned by telephone in order to resolve such informalities.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number 571-273-8300 to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 this 23rd day of December, 2005.